## REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 1-28 were pending in this application. Non-elected Claims 24-28 had been withdrawn from consideration and have now been cancelled without prejudice. Claims 6, 10, and 12 have also been cancelled without prejudice. Claims 4 and 15 have been amended to better define the scope of the claimed invention. New Claims 29-34 have been added. Applicant thanks the Examiner for indicating the allowability of Claims 14 and 16-19.

The drawings were objected to for not showing every feature of the claimed invention. New Figures 7 and 8 are proposed herein in response to the objection.

Claims 2, 4, and 15 stand rejected under 35 U.S.C. 112, second paragraph. In Claim 2, the Examiner asserts that the meaning of the symbol "□" is unclear. Applicant replies that the symbol represents a square. The units of the claimed resistance are milliohms per square, which is well known in the industry as a measure of sheet resistance. Claims 4 and 15 have been amended in response to the rejection.

Claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki, et al. (U.S. 5,973,554). Claim 1 includes the feature of " a network of power distribution lines deposited on the surface of said chip over active components of said circuit." Yamasaki does not disclose such a feature. Note that element 70 in Yamasaki's Figures 2B and 3 is a capacitor, not an active component. Therefore, Applicant respectfully submits that Claim 1 is patentable over Yamasaki.

Claims 2 and 3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki. Claims 2 and 3 depend from Claim 1, which, as argued above, includes features not disclosed or suggested in Yamasaki.

Claims 4-8, 10-12, 15, 20, 21, and 23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki, in view of Tani (U.S. 5,468,993). Claim 4 includes the feature of "electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having an outermost film of non-corrodible, metallurgically attachable metal." As noted above, Yamasaki does not disclose or suggest such a feature. Yamasaki's element 70 is a capacitor, not an active component. In addition, Claim 4 includes the feature of " a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground." Yamasaki's leadframe 2, 61 is a so-called "lead-on-chip" style in which no die mount pad is used. Tani is therefore nonanalogous art and one skilled in the art would receive no motivation from the cited references for a combination of Tani's traditional leadframe die mount pad with that of Yamasaki's lead-on-chip style leadframe. Therefore, Applicant respectfully submits that Claim 4 is patentable over the cited references. Claims 5-8, 10-12, 15, 20, 21, and 23 depend from Claim 4 and are therefore patentable for at least the reasons presented above.

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki in view of Tani in view of Applicant's Admitted Prior Art. Applicant's Admitted Prior Art does not cure the deficiencies of Yamasaki and Tani. Therefore, Applicant respectfully submits that Claim 4 is patentable over the cited combination of references. Claim 9 depends from Claim 4 and is therefore patentable over the cited combination for at least the reasons presented above.

Claims 13, 20, and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki in view of Tani in view of Wolf, et al. Claims 13, 20, and 22 depend from Claim 4, which as indicated above, is patentable over Yamasaki in view of Tani. Wolf does not cure the deficiencies of Yamasaki and Tani with respect to Claim 4. Therefore, Applicant respectfully submits that Claims 13, 20, and 22 are patentable over the references of record for at least the reasons presented above.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-23 and 29-34. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**In the Specification:**

*On page 5, in the second paragraph:*

In the recent U.S. Patent Application number 09/975,630, filed on 10/12/2001 (Taylor R. Efland "Circuit Structure Integrating the Power Distribution Functions of Circuits and Leadframes into the Chip Surface") [(Efland, TI-31678)], an integrated circuit (IC) chip is described, which is mounted on a leadframe and has a network of power distribution lines deposited on the surface of the chip so that these lines are located over active components of the IC. The lines are connected vertically by metal-filled vias to selected active IC components below the lines, and also by conductors to segments of the leadframe. The present invention is related to this disclosure.

*On page 11, in the Section titled "Brief Description of the Drawings":*

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified perspective and cross sectional view of a power distribution line over an integrated circuit (IC) fabricated in a semiconductor chip attached to a leadframe mount pad, with an electrical conductor connecting to a leadframe segment, according to an embodiment of the invention.

FIG. 2 is a simplified perspective and cross sectional view of a portion of a power distribution line, with connecting member attached, according to a preferred embodiment of the invention.

FIG. 3 is a schematic top view of an IC indicating the positioning of contact pads according to known technology.

FIG. 4 illustrates schematically the positioning of contact pads, with emphasis on morphing a plurality of power supply contact pads into a power distribution line, according to an embodiment of the invention.

FIG. 5A is a schematic and simplified top view of a portion of an IC chip, schematically indicating electrical power connection in prior art, and resulting electrical resistance in current flow.

FIG. 5B is a schematic and simplified top view of a portion of an IC chip, schematically indicating electrical power connection according to the invention, and resulting electrical resistance in current flow.

FIG. 6 is a schematic diagram of individualized power distribution lines deposited over an active IC for lowering electrical parasitics.

FIG. 7 is a simplified perspective and cross sectional view of a power distribution line over an integrated circuit (IC) fabricated in a semiconductor chip with a solder ball mounted to the distribution line through an opening in a solder mask layer.

FIG. 8 is a simplified perspective and cross sectional view of a power distribution line over an integrated circuit (IC) fabricated in a semiconductor chip with a ribbon connecting the distribution line to a leadframe segment.

*On page 12, in the first paragraph:*

The present invention is related to U.S. Patent Applications # 08/959,410, filed on 10-28-1997, # 09/611,623, filed on 07-07-2000 (Shen et al., "Integrated Circuit with Bonding Layer over Active Circuitry"), # 60/221,051, filed on 07-27-2000 [200] (Efland et al., "Integrated Power Circuits with Distributed Bonding and Current Flow"), and U.S. Patent Application number 09/975,630, filed on 10/12/2001 (Taylor R. Efland [TI-31678 (Efland], "Circuit Structure Integrating the Power Distribution Functions of Circuits and Leadframes into the Chip Surface"), which are herewith incorporated by reference.

*On page 17, in the first paragraph:*

If outermost layer 165 is selected so that it is solderable, a solder ball (700 in Figure 7) can be attached to it by standard reflow techniques. However, it was described in the abovecited U.S. Patent Application # 09/611,623 that it is often advisable to employ an additional solder mask 702 or polyimide layer [(not

shown in Figure 1)] with an opening 704 for each solder ball. This technique keeps the flip-chip bump in a defined area and shape during bump formation and subsequent attachment to an external package or board.

*On page 18, in the first paragraph:*

Outermost metal layer 165 is equally well suited for wedge bonding, involving ribbons (800 in Figure 8).

**In the Claims:**

4. (amended) A semiconductor device wherein electrical parasitics are minimized by individualized power distributors deposited over active integrated circuit components, comprising:

a semiconductor chip having first and second surfaces;

an integrated circuit fabricated on said first chip surface, said circuit having active components, contact pads, at least one metal layer, and being protected by a mechanically strong, electrically insulating overcoat having a plurality of metal-filled vias to contact said at least one metal layer[, and a plurality of windows to expose circuit contact pads];

electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having an outermost film of non-corrodible, metallurgically attachable metal;

said network patterned to distribute power current while minimizing parasitic electrical losses between said network and said active components;

said network further patterned to minimize silicon real estate consumed by power interconnections between said active components;

a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground;

said second chip surface attached to said chip mount pad;

electrical conductors connecting said [chip] contact pads with said first plurality of segments; and

electrical conductors connecting said network lines with said second plurality of segments.

6. (cancelled)

10. (cancelled)

12. (cancelled)

15. (amended) The device according to Claim 4 wherein said electrical conductors are selected from a group comprising [metallurgical attachment comprises] wire ball and stitch bonding, ribbon bonding, and soldering.

24-28 (cancelled)

Please add the following new claims:

29. (new) An integrated circuit chip mounted on a leadframe, said leadframe having a plurality of segments, comprising:

a network of power distribution lines deposited on the surface of said chip over active components of said circuit;

said lines comprising a stack including a stress-absorbing metal film;

said lines connected vertically to said components by metal-filled vias, and also to said segments by conductors; and

the majority of said lines patterned as straight lines between said vias and said conductors.

30. (new) The device of Claim 29, wherein said stack including a stress-absorbing metal film comprises an outermost metallurgically attachable film.

31. (new) The device of Claim 29, wherein said stack including a stress-absorbing metal film comprises a layer of seed metal, a stress-absorbing metal layer on said seed metal layer, and an outermost metallurgically attachable metal layer.

32. (new) The device of Claim 31, wherein said stress-absorbing metal layer comprises at least one layer selected from a group consisting of copper, nickel, aluminum, and alloys thereof.

33. (new) The device of Claim 31, wherein said seed metal is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof.

34. (new) The device according to Claim 31, wherein said outermost metal layer is selected from a group consisting of pure or alloyed aluminum, gold, palladium, silver and platinum.

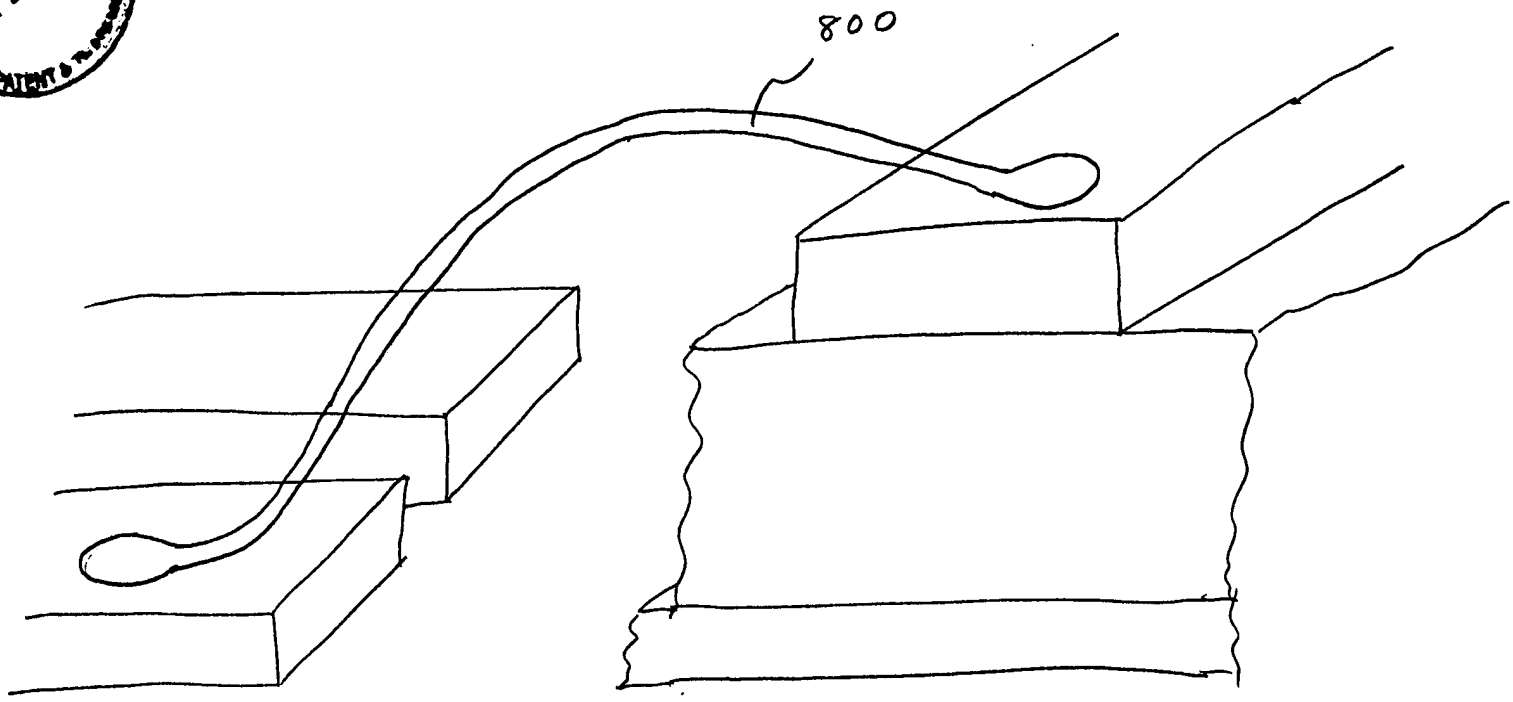


Fig. 8

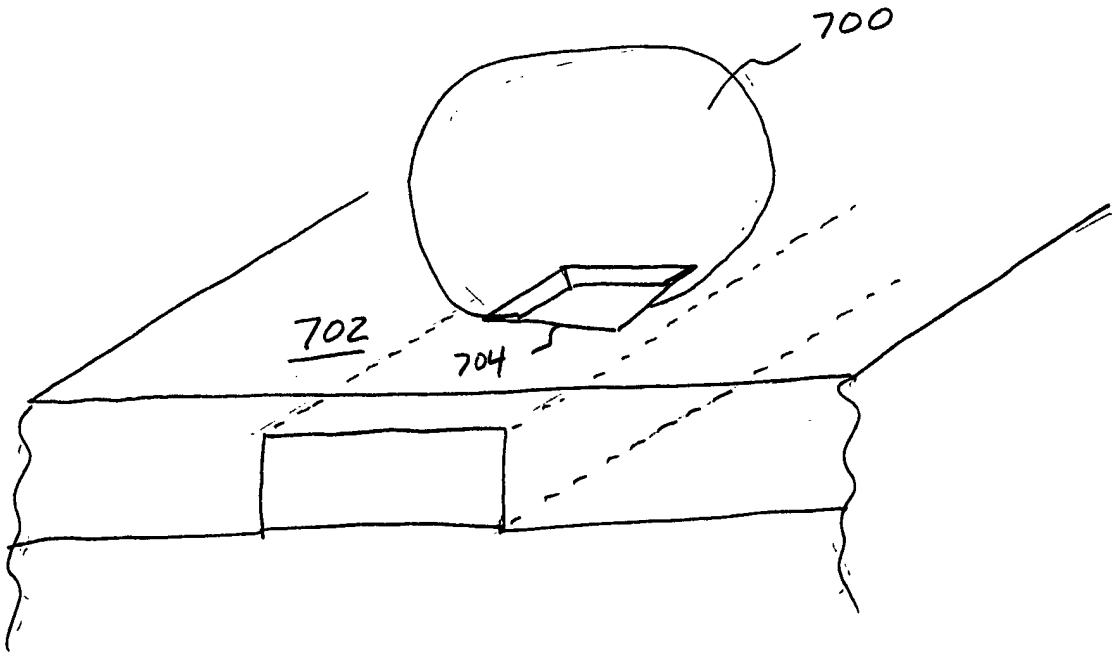


Fig. 7

Proposed Drawing Modifications